UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,880	03/03/2004	Satoru Akiyama	500.43581X00	4729

20457 7590 08/10/2007

ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-3873

EXAMINER	
TRAN, DENISE	

ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
08/10/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

MN

Office Action Summary	Application No.	Applicant(s)	
	10/790,880	AKIYAMA ET AL.	
	Examiner	Art Unit	
	Denise Tran	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3, 5-12, 20-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-12 and 20-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The applicant's amendment filed 5/23/07. Claims 1-3, 5-12, and newly added claims 20-28 are presented for examination. Claims 4 and 13-19 have been canceled.

2. Content of Specification

(a) Title of the Invention: See 37 CFR 1.72(a) and MPEP § 606. The title of the invention should be placed at the top of the first page of the specification unless the title is provided in an application data sheet. The title of the invention should be brief but technically accurate and descriptive, preferably from two to seven words may not contain more than 500 characters.

(b) Cross-References to Related Applications: See 37 CFR 1.78 and MPEP § 201.11.

(c) Statement Regarding Federally Sponsored Research and Development: See MPEP § 310.

(d) The Names Of The Parties To A Joint Research Agreement: See 37 CFR 1.71(g).

(e) Incorporation-By-Reference Of Material Submitted On a Compact Disc: The specification is required to include an incorporation-by-reference of electronic documents that are to become part of the permanent United States Patent and Trademark Office records in the file of a patent application. See 37 CFR 1.52(e) and MPEP § 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text were permitted as electronic documents on compact discs beginning on September 8, 2000.

(f) Background of the Invention: See MPEP § 608.01(c). The specification should set forth the Background of the Invention in two parts:

(1) Field of the Invention: A statement of the field of art to which the invention pertains. This statement may include a paraphrasing of the applicable U.S. patent classification definitions of the subject matter of the claimed invention. This item may also be titled "Technical Field."

(2) Description of the Related Art including information disclosed under 37 CFR 1.97 and 37 CFR 1.98: A description of the related art known to the applicant and including, if applicable, references to specific related art and problems involved in the prior art which are solved by the applicant's invention. This item may also be titled "Background Art."

(g) Brief Summary of the Invention: See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention.

(h) Brief Description of the Several Views of the Drawing(s): See MPEP § 608.01(f). A reference to and brief description of the drawing(s) as set forth in 37 CFR 1.74.

(i) Detailed Description of the Invention: See MPEP § 608.01(g). A description of the preferred embodiment(s) of the invention as required in 37 CFR 1.71. The description should be as short and specific as is necessary to describe the invention adequately and accurately. Where elements or groups of elements, compounds, and processes, which are conventional and generally widely known in the field of the invention described and their exact nature or type is not necessary for an understanding and use of the invention by a person skilled in the art, they should not be described in detail. However, where particularly complicated subject matter is involved or where the elements, compounds, or processes may not be commonly or widely known in the field, the specification should refer to another patent or readily available publication which adequately describes the subject matter.

(j) Claim or Claims: See 37 CFR 1.75 and MPEP § 608.01(m). The claim or claims must commence on separate sheet or electronic page (37 CFR 1.52(b)(3)). Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. See 37 CFR 1.75 and MPEP § 608.01(i)-(p).

(k) Abstract of the Disclosure: See MPEP § 608.01(f). A brief narrative of the disclosure as a whole in a single paragraph of 150 words or less commencing on a separate sheet following the claims. In an international application which has entered the national stage (37 CFR 1.491(b)), the applicant need not submit an abstract commencing on a separate sheet if an abstract was published with the international application under PCT Article 21. The abstract that appears on the cover page of the pamphlet published by the International Bureau (IB) of the World Intellectual Property Organization (WIPO) is the abstract that will be used by the USPTO. See MPEP § 1893.03(e).

(l) Sequence Listing, See 37 CFR 1.821-1.825 and MPEP §§ 2421-2431. The requirement for a sequence listing applies to all sequences disclosed in a given application, whether the sequences are claimed or not. See MPEP § 2421.02.

3. The disclosure is objected to because of the following informalities: pages 4-6 should be "Background Art."

Appropriate correction is required.

4. Claims 9 and 25 are objected to because of the following informalities: "said flag" line 1 should be a flag. Appropriate correction is required.

5. The indicated allowability of claims 4-5 and 7-9 are withdrawn in view of the reference(s) to Akiyama et al., US 6848035 and Akiyama et al., US 2003/0033492.

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140

F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claim 20 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6848035 in view of Ooishi, US 2004/0027857. Claim 1 of U.S. Patent No. 6848035 teaches a semiconductor device comprising:

a plurality of memory banks, each having a plurality of memory cells; and

a cache memory for mediating an access to said plurality of memory banks from the outside; and

an internal data bus for coupling said cache memory to said memory banks; and

a plurality of data input/output nodes for inputting/outputting data from/to the outside,

wherein said cache memory has a cache line comprised of a plurality of sublines, and

A=N.B is satisfied, where N is the number of said plurality of sublines, A is a bus width of said internal data bus, and B is a bus width of said external data bus. Claim 1

of U.S. Patent No. 6848035 does not explicitly show the use of slower in a write operation than in a read operation and a cache memory having a number of way equal to or larger than a value determined by a ratio (m/n) of a write cycle (m) of said memory cells to a read cycle (n) of said memory cells. Ooishi teaches the use of slower in a write operation than in a read operation (e.g., [0085] [0101]) and a cache memory having a number of way equal to or larger than a value (i.e., 1 or 2 or N ways cache; e.g., [0220])) determined inherently by a ratio (m/n) of a write cycle (m) of said memory cells to a read cycle (n) of said memory cells (e.g., fig. 13, [0195]-[0202], a read cycle n and write cycle m at any clock cycle from 1 to 7, 0/2, 1/3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Ooishi into the system of U.S. Patent No. 6848035 because it would prevent an increase in the chip size and reduce a cost and allow faster access time.

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-3, 5-12 and 20-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama et al., US 2003/0033492, (hereinafter Akiyama), in view of Atwood et al., "SESO Memory: a CMOS Compatible High Density Embedded Memory

technology for Mobile Applications, " 2002, Symposium on VLSI Circuit Digest of Technical Papers pp. 154-155, (2000) (hereinafter Atwood).

Claim 1, Akiyama teaches a semiconductor device comprising:

a plurality of memory banks, each having a plurality of memory cells (e.g., figs. 1, 7, el. bank0-bank4; [0003]); and

a cache memory for mediating an access to the memory from the outside (e.g., figs 1, 6-7, cachemen; [0030]; [0039]), said cache memory having a number of way equal to or larger than a value (i.e., 1 or 2 ways; e.g., figs 1, 6-7, cachemen; [0074]; [0086]) determined inherently by a ratio (m/n) of a write cycle (m) of said memory cells to a read cycle (n) of said memory cells (e.g., fig. 8, , a read cycle n =1 or 2 and write cycle m = 1; m/n = 1/1 = 1 or m/n= 1/2); and

when first data is written into said semiconductor device from the outside, wherein said cache memory does not hold an address at which said first data is to be written (e.g., [0056]), data held in an associated entry of said cache memory is written back to one of said plurality of memory banks (e.g., [0056]), and said first data is written into said cache memory (e.g., [0056]).

Akiyama does not explicitly show memory cells which are slower in a write operation than in a read operation. Atwood teaches memory cells which are slower in a write operation than in a read operation (e.g., page 154, column 2, paragraph 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Atwood into the system of Akiyama because it would provide a high density, low power embedded memory.

Claim 20, Akiyama teaches a semiconductor device comprising:

a plurality of memory banks, each having a plurality of memory cells (e.g., figs. 1, 7, el. bank0-bank4; [0003]); and

a cache memory for mediating an access to the memory from the outside (e.g., figs 1, 6-7, cachemen; [0030]; [0039]), said cache memory having a number of way equal to or larger than a value (i.e., 1 or 2 ways; e.g., figs 1, 6-7, cachemen; [0074]; [0086]) determined inherently by a ratio (m/n) of a write cycle (m) of said memory cells to a read cycle (n) of said memory cells (e.g., fig. 8, , a read cycle n =1 or 2 and write cycle m = 1; m/n = 1/1 = 1 or m/n= 1/2); and

an internal data bus for coupling said cache memory to said memory banks (e.g., page 11, claim 5); and

a plurality of data input/output nodes for inputting/outputting data from/to the outside (e.g., page 11, claim 5),

wherein said cache memory has a cache line comprised of a plurality of sublines (e.g., page 11, claims 1 and 5), and

A=N.B is satisfied, where N is the number of said plurality of sublines, A is a bus width of said internal data bus, and B is a bus width of said external data bus (e.g., page 11, claim 5).

Akiyama does not explicitly show memory cells which are slower in a write operation than in a read operation. Atwood teaches memory cells which are slower in a write operation than in a read operation (e.g., page 154, column 2, paragraph 2). It

would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Atwood into the system of Akiyama because it would provide a high density, low power embedded memory.

Claims 2-3, 5 and 21-22, Akiyama teaches said cache memory has a plurality of sets corresponding to the number of ways, and each of said plurality of sets has a capacity for storing whole data stored in one of said plurality of memory banks (e.g., [0090]); when said cache memory holds data corresponding to an access to said semiconductor device from the outside, the data is communicated from said cache memory (e.g.,[0030]); and when data is written back to one of said plurality of memory banks, wherein a first memory bank included in said plurality of memory banks cannot accept an access from the outside, the data is written back to a second memory bank included in said plurality of memory banks (e.g., [0058]).

Claims 6-7 and 23, Akiyama teaches a plurality of data input/output nodes for inputting/outputting data to/from the outside, wherein each said data input/output node has a data width equal to a data width of an external data bus for inputting/outputting information to/from said semiconductor device; an internal data bus for coupling said cache memory to said memory banks (e.g., page 11, claim 5; page 3, [0027]); wherein said cache memory has a cache line comprised of a plurality of sublines, and A=N. B is satisfied, where N is the number of said plurality of sublines, A is a bus width of said internal data bus, and B is a bus width of said external data bus (e.g., page 11, claim 5);

said cache memory has a plurality of flags each associated with one subline for managing data held thereon (e.g., fig. 3A, v0-v3, D0-D3);

Claims 8-9, 12, 24-25, and 28, Akiyama teaches when said flag indicates data on said subline as invalid, a write-back operation is not performed from said cache memory to said memory bank (e.g., fig. 2B, S205; [0057]-[0058]); when said flag indicates that data on said subline has been updated, a data write operation is not performed from said memory bank to said cache memory (e.g., [0058]); and wherein said cache memory comprises SRAM memory cells [e.g., 0027].

Claims 10-11 and 26-27, Akiyama teaches wherein said cache memory comprises SRAM memory cells [0027]. Akiyama does not explicitly show wherein each said memory cell is either a SESO (Single Electron Shut Off) memory cell or a phase change memory cell. Atwood teaches memory cell is either a SESO (Single Electron Shut Off) memory cell or a phase change memory cell (e.g., page 154, column 2, paragraph 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Atwood into the system of Akiyama because it would provide a high density, low power embedded memory.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (571) 272-4189. The examiner can normally be reached on Monday and Thursday from 8:45 a.m. to 5:15 p.m.. The examiner can also be reached on alternate Friday

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah, can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Denise Tran

8/4/07